IN THE CLAIMS

Please amend the claims as follows:

1. (Currently Amended) A duty cycle adjust circuit comprising:

a first programmable logic circuit to output ~~one of~~ a plurality of variable incremental high logic signals ~~upon receiving a first control signal based on one of a predetermined amount of incremental high signals from~~ , the incremental logic signals to increment edges of a high signal of an input clock signal in accordance with a set of first control signals, ~~or~~ and to output ~~one of~~ a plurality of variable decremental high logic signals ~~upon receiving a second control signal based on one of a predetermined amount of decremental high signals from~~ , the decremental logic signals to decrement edges of the high signal of the input clock signal in accordance with the first control signals;

a second programmable logic circuit to output an incremented high logic signal ~~upon receiving a third control signal~~ or to output a decremented high logic signal upon receiving a ~~fourth~~ second control signal;

a positive variable duty cycle adjust circuit to couple to an input clock terminal (CLK IN) to receive the input clock signal and the incremental high logic signals and to output ~~one of a plurality of~~ an incremented duty cycle adjusted clock signal~~s~~, the clock signal having ~~an incremented~~ a high signal incremented from the high signal of the input clock signal as a function of the first control signals;

a negative variable duty cycle adjust circuit to couple to couple to the CLK IN to receive the input clock signal and the decremental high logic signals and to output ~~one of a plurality of~~ a decremented duty cycle adjusted clock signals, the clock signal having a ~~decremented~~ high signal decremented from the high signal of the input clock signal as a function of the ~~second~~ first control signals; and

an output module to receive the incremented and decremented high logic signals and the incremented and decremented duty cycle adjusted clock signals, and to couple to an output clock terminal (CLK OUT) to output an adjusted clock signal having ~~one of the plurality of~~ an incremented or decremented duty cycle clock signals as a function of the ~~incremented or decremented high logic signal, respectively~~ second control signal.

2. (Original) The circuit of claim 1, further comprising:

an oscillator coupled to the CLK IN to generate the input clock signal having the high signal and a low signal within a clock cycle.

3. (Currently Amended) The circuit of claim 1, wherein the first programmable logic circuit comprises:

a plurality of memory elements associated with the ~~predetermined amount of~~ incremental and decremental high logic signals, wherein each memory element has an input and an output, ~~wherein~~ each input to couple to receive an associated first control signal; and

a plurality of inverters, wherein each inverter has an input and an output, wherein the input of each inverter is coupled to the output of an associated memory element, wherein the output of the inverter is coupled to the positive variable duty cycle adjust circuit and the negative variable duty cycle adjust circuit.

4. (Original) The circuit of claim 3, wherein the positive variable duty cycle adjust circuit comprises:

a plurality of duty cycle incremental adjust circuits associated with the plurality of incremental high signals, wherein each duty cycle incremental adjust circuit comprises a plurality of NAND gates.

5. (Original) The circuit of claim 4, wherein each plurality of NAND gates of the plurality of duty cycle incremental adjust circuits comprise:

a first NAND gate having first and second inputs and an output, wherein the first input of the first NAND gate is coupled to the output of an associated memory element of the first programmable logic circuit and the input of the associated inverter of the first programmable logic circuit, and wherein the second input of the first NAND gate to couple to the CLK IN;

a second NAND gate having first and second inputs and an output, wherein the first input of the second NAND gate is to coupled to a power source V_{cc}, and wherein the second input of the second NAND gate is coupled to the output of the first NAND gate; and

a third NAND gate having first and second inputs and an output, wherein the first input of the third NAND gate is coupled to the output of the associated inverter of the first programmable logic circuit, wherein the second input of the third NAND gate is coupled to the output of the second NAND gate, and wherein the output of the third NAND gate is coupled to a first input of a second NAND gate of a subsequent duty cycle incremental adjust circuit.

6. (Original) The circuit of claim 5, wherein each duty cycle incremental adjust circuit of the positive variable duty cycle adjust circuit further comprises:

a capacitor coupled to each plurality of NAND gates of duty cycle incremental adjust circuit such that one end of the capacitor is coupled between an output of the second NAND gate and the second input of the third NAND gate and the other end of the capacitor to couple to ground (GND).

7. (Original) The circuit of claim 4, wherein the negative variable duty cycle adjust circuit comprises:

a plurality of associated duty cycle decremental adjust circuits associated with the plurality of decremental high signals, wherein each associated duty cycle decremental adjust circuit comprises a plurality of NAND gates.

8. (Original) The circuit of claim 7, wherein each plurality of NAND gates of the plurality of the negative variable duty cycle adjust circuit comprise:

a first NAND gate having first and second inputs and an output, wherein the first input of the first NAND gate to couple to the CLK IN, and wherein the second input of the first NAND gate is coupled to the output of the associated memory element of the first programmable logic circuit and the input of the associated inverter of the first programmable logic circuit;

a second NAND gate having first and second inputs and an output, wherein the first input of the second NAND gate is coupled to the output of the first NAND gate, and wherein the second input of the second NAND gate is to couple to the power source V_{cc}; and

a third NAND gate having first and second inputs and an output, wherein the first input of the third NAND gate is coupled to the output of the second NAND gate, wherein the second

input of the second NAND gate is coupled to the output of the associated inverter of the first programmable logic circuit, and wherein the output of the third NAND gate is coupled to a second input of a second NAND gate of a subsequent associated duty cycle decremental adjust circuit.

9. (Original) The circuit of claim 8, wherein the negative variable duty cycle adjust circuit further comprises:

a plurality of capacitors, wherein each capacitor is connected to each of the associated duty cycle decremental adjust circuits such that one end of the capacitor is coupled between the output of the third NAND gate and the second input of the second NAND gate of the subsequent duty cycle decremental adjust circuit, and the other end of the capacitor is to couple to GND.

10. (Original) The circuit of claim 8, wherein the second programmable logic circuit comprises:

a memory element having an input and an output, wherein the input of the memory element to couple to receive the second control signal; and

an inverter coupled to the memory element of the second programmable logic circuit, wherein the inverter of the second programmable logic circuit has an input and an output, wherein the input of the inverter of the second programmable logic circuit is coupled to the output of the memory element of the second programmable logic circuit, wherein the inverter to output the incremented high logic signal or the decremented high logic signal as a function of the second control signal.

11. (Original) The circuit of claim 10, wherein the output module comprises:

a duty cycle incremental select circuit, wherein the duty cycle incremental select circuit comprises a plurality of NAND gates coupled to the output of the inverter of the second programmable logic circuit, the positive variable duty cycle adjust circuit, and the output module; and

an associated duty cycle decremental adjust circuit, wherein the associated duty cycle decremental adjust circuit comprises a plurality of NAND gates coupled to the output of the

inverter of the second programmable logic circuit, the negative variable duty cycle adjust circuit, and the output module.

12. (Original) The circuit of claim 11, wherein the plurality of NAND gates of the duty cycle incremental select circuit of the output module comprises:

a first NAND gate having first and second inputs and an output, wherein the first input of the first NAND gate is coupled to the input of the inverter and the output of the memory element of the second programmable logic circuit and wherein the second input to couple to the CLK IN;

a second NAND gate having first and second inputs and an output, wherein the first input of the second NAND gate is coupled to the output of a third NAND gate of a precedent duty cycle incremental select circuit and wherein the second input of the second NAND gate is coupled to the output of the first NAND gate; and

a third NAND gate having first and second inputs and an output, wherein the first input of the third NAND gate is coupled to the output of the inverter of the second programmable logic circuit, and the second input of the third NAND gate is coupled to the output of the second NAND gate.

13. (Original) The circuit of claim 12, wherein the duty cycle incremental select circuit of the second programmable logic circuit further comprises:

a capacitor coupled between the output of the second NAND gate and the second input of the third NAND gate of the output module.

14. (Original) The circuit of claim 12, wherein the plurality of NAND gates of the associated duty cycle decremental adjust circuit of the output module comprises:

a first NAND gate having first and second inputs and an output, wherein the first input of the NAND gate to couple to the CLK IN and wherein the second input of the first NAND gate is coupled to the output of the memory element and the input of the inverter of the second programmable logic circuit;

a second NAND gate having first and second inputs and an output, wherein the first input of the second NAND gate is coupled to the output of the first NAND gate, and wherein the

second input of the second NAND gate is coupled to output of a third NAND gate of a precedent plurality of NAND gates of the duty cycle decremental select circuit; and

a third NAND gate having first and second inputs and an output, wherein the first input of the third NAND gate is coupled to the output of the second NAND gate, and wherein the second input of the third NAND gate is coupled to the output of the inverter of the second programmable logic circuit.

15. (Original) The circuit of claim 14, wherein the associated duty cycle decremental adjust circuit of the output module comprises:

a capacitor coupled between the output of the third NAND gate and the output module.

16. (Original) The circuit of claim 15, wherein the output module further comprises:

a NAND gate having first and second inputs and an output, wherein the first input of the NAND gate of the output module is coupled to the output of the third NAND gate of the duty cycle incremental select circuit of the second programmable logic circuit, wherein the second input of the NAND gate of the output module is coupled to the output of the third NAND gate of the associated duty cycle decremental adjust circuit of the second programmable logic circuit, and wherein the output of the NAND gate of the output module to couple to the CLK OUT.

17. (Currently Amended) A circuit comprising:

a first edge-triggered circuit to output ~~one of~~ a plurality of variable incremental or decremental high logic signals ~~upon receiving a first~~ set of ~~control signals based on one of a plurality of predetermined amount of incremental~~ to increment separations between a raising edge and a falling edge of an input clock signal or ~~upon receiving a second control signal based on one or a plurality of predetermined amount of decremental~~ to decrement separations between the raising edge and the falling edge of the input clock signal in accordance with a set of first control signals;

a second edge-triggered circuit to output an incremented high logic signal or to output a decremented high logic signal ~~upon receiving a third control signal or a fourth~~ in accordance with a second control signal~~, respectively~~;

a positive variable duty cycle adjust circuit to couple to an input clock terminal (CLK IN) to receive the input clock signal and the incremental high logic signals and to output an incremented duty cycle adjusted clock signal, the clock signal having one of ~~the~~ a plurality of predetermined ~~amount of~~ incremental separations between the raising edge and the falling edge of the input clock signal as a function of ~~the one of~~ the plurality of variable incremental high logic signals;

a negative variable duty cycle adjust circuit to couple to the CLK IN to receive the input clock signal and the decremental high logic signals and to output a decremented duty cycle adjusted clock signal, the clock signal having one of ~~the~~ a plurality of predetermined ~~amount of~~ decremental separations between the raising edge and the falling edge of the input clock signal as a function of ~~the one of~~ the plurality of variable decremental high logic signals; and

an output module to receive the incremented and decremented high logic signals and the incremented and decremented duty cycle adjusted clock signals, and to couple to an output clock terminal (CLK OUT) to output the incremented duty cycle adjusted clock signal or the decremented duty cycle adjusted clock signal as a function of the incremented high logic signal or the decremented high logic signal, respectively.

18. (Original) The circuit of claim 17, further comprising;

an oscillator coupled to the CLK IN to generate the input clock signal having the high logic signal and a low logic signal in a clock cycle.

19. (Currently Amended) The circuit of claim 17, wherein the first edge-triggered circuit comprises:

a plurality of registers associated with the ~~predetermined amount of~~ incremental and decremental high logic signals, wherein each register has an input and an output, ~~wherein~~ each input to couple to receive an associated first control signal from the set of first control signals ~~or an associated second control signal~~; and

a plurality of inverters, wherein each inverter has an input and an output, wherein the input of each inverter is coupled to the output of an associated register, wherein the output of the inverter is coupled to the positive and negative variable duty cycle adjust circuits.

20. (Currently Amended) The circuit of claim 19, wherein the plurality of registers comprises a plurality of flip-flop circuits, wherein each flip-flop circuit to store the ~~received~~ associated first control signal ~~or the second control signal~~, ~~wherein~~ the associated first control signals corresponding to ~~is based on~~ a ~~first~~ programmed instruction ~~and the second control signal is based on a second programmed instruction~~.

21. (Original) The circuit of claim 17, wherein the positive variable duty cycle adjust circuit comprises:

a plurality of multiple NAND gates to increase separation between the raising and falling edges, wherein each multiple NAND gates comprise:

a first NAND gate having first and second inputs and an output, wherein the first input of the first NAND gate is coupled to the output of the associated register of the first edge-triggered circuit and the input of the associated inverter of the first edge-triggered circuit, and wherein the second input of the first NAND gate to couple to the CLK IN;

a second NAND gate having first and second inputs and an output, wherein the first input of the second NAND gate is coupled to the CLK IN is to coupled to a power source V_{cc}, and wherein the second input of the second NAND gate is coupled to the output of the first NAND gate; and

a third NAND gate having first and second inputs and an output, wherein the first input of the third NAND gate is coupled to the output of the associated inverter of the first edge-triggered circuit, wherein the second input is coupled to the output of the second NAND gate, and wherein the output of the third NAND gate is coupled to a first input of a second NAND gate of a subsequent multiple NAND gates.

22. (Original) The circuit of claim 21, wherein the positive variable duty cycle adjust circuit further comprises:

a plurality of capacitors, wherein each capacitor is connected to each multiple NAND gates of the positive variable duty cycle adjust circuit such that one end of the capacitor is

coupled between an output of the second NAND gate and the second input of the third NAND gate of the multiple NAND gates and the other end of the capacitor to couple to ground (GND).

23. (Original) The circuit of claim 17, wherein the negative variable duty cycle adjust circuit comprises:

a plurality of associated multiple NAND gates, wherein each of the multiple NAND gates comprises:

a first NAND gate having first and second inputs and an output, wherein the first input of the first NAND gate to couple to the CLK IN, and wherein the second input of the first NAND gate is coupled to the output of the associated register of the first edge-triggered circuit and the input of the associated inverter of the first edge-triggered circuit;

a second NAND gate having first and second inputs and an output, wherein the first input of the second NAND gate is coupled to output of the first NAND gate, and wherein the second input of the second NAND gate is to couple to the power source V_{cc}; and

a third NAND gate having first and second inputs and an output, wherein the first input of the third NAND gate is coupled to the output of the second NAND gate, wherein the second input of the second NAND gate is coupled to the output of the associated inverter of the first edge-triggered circuit, and wherein the output of the third NAND gate is coupled to a second input of a second NAND gate of a subsequent multiple NAND gates of the plurality of multiple NAND gates.

24. (Original) The circuit of claim 23, wherein the negative variable duty cycle adjust circuit further comprises:

a plurality of capacitors, wherein each capacitor is connected to each of the multiple NAND gates of the negative variable duty cycle adjust circuit such that one end of the capacitor is coupled between an output of the third NAND gate and the second input of the second NAND gate of the subsequent multiple NAND gates, and the other end of the capacitor is to couple to GND.

25. (Original) The circuit of claim 17, wherein the second edge-triggered circuit comprises:

a register having an input and an output, wherein the input of the register to couple to receive the second control signal based on a desired incremented high signal or a decremented low signal; and

an inverter coupled to the register of the second edge-triggered circuit, wherein the inverter of the second edge-triggered circuit has an input and an output, wherein the input of the inverter of the second edge-triggered circuit is coupled to the out put of the register of the second edge-triggered circuit, wherein the output of the inverter to output the incremented high logic signal or the decremented high logic signal as a function of the second control signal.

26. (Original) The circuit of claim 25, wherein the output module comprises:

first multiple NAND gates to coupled to the output of the inverter of the second edge-triggered circuit, the positive variable duty cycle adjust circuit, and the output module;

second multiple NAND gates coupled to the output of the inverter of the second edge-triggered circuit, the negative variable duty cycle adjust circuit, and the output module; and

an adjusted clock signal NAND gate having first and second inputs and an output, wherein the output of the adjusted clock signal NAND gate is to couple to CLK OUT to provide one of the plurality of adjusted clock signals.

27. (Original) The circuit of claim 26, wherein the first multiple NAND gates of the output module further comprises:

a first NAND gate having first and second inputs and an output, wherein the first input of the first NAND gate is coupled to the input of the inverter and the output of the register of the second edge-triggered circuit and wherein the second input to couple to the CLK IN;

a second NAND gate having first and second inputs and an output, wherein the first input of the second NAND gate is coupled to the output of the third NAND gate of the precedent first multiple NAND gates and wherein the second input of the second NAND gate is coupled to the output of the first NAND gate; and

a third NAND gate having first and second inputs and an output, wherein the first input of the third NAND gate is coupled to the output of the inverter of the second edge-triggered circuit, the second input of the third NAND gate is coupled to the output of the second NAND gate, and wherein the output of the third NAND gate is coupled to the first input of the adjusted clock signal NAND gate.

28. (Original) The circuit of claim 27, wherein the first multiple NAND gates of the output module further comprises:

a capacitor coupled between the output of the second NAND gate and the second input of the third NAND gate.

29. (Original) The circuit of claim 27, wherein the second multiple NAND gates of the output module comprises:

a first NAND gate having first and second inputs and an output, wherein the first input of the first NAND gate to couple to the CLK IN and wherein the second input of the first NAND gate is coupled to the output of the register and the input of the inverter of the second edge-triggered circuit;

a second NAND gate having first and second inputs and an output, wherein the first input of the second NAND gate is coupled to the output of the first NAND gate, wherein the second input of the second NAND gate is coupled to output of a third NAND gate of a precedent second multiple NAND gates; and

a third NAND gate having first and second inputs and an output, wherein the first input of the third NAND gate is coupled to the output of the second NAND gate, wherein the second input of the third NAND gate is coupled to the output of the inverter of the second edge-triggered circuit, and wherein the output of the third NAND gate is coupled to the second input of the adjusted clock signal NAND gate.

30. (Original) The circuit of claim 29, wherein the second multiple NAND gates of the output module further comprises:

a capacitor coupled between the output of the third NAND gate and the second input of the adjusted clock signal NAND gate.

31. (Currently Amended) A method of adjusting duty cycle of an input clock signal in an integrated circuit, comprising:

inputting a first programmed instruction for selecting one of a plurality of incremented or decremented separations between a raising edge and a falling edge of a clock signal into the integrated circuit device;

generating a set of first control signals ~~or a second control signal~~ as a function of the first programmed instruction;

generating one of a plurality of incremented or decremented duty cycle adjusted clock signals by incrementing or decrementing a separation between the raising edge and the falling edge of the input clock signal as a function of the first control signals;

inputting a second programmed instruction for selecting to output the generated one of the plurality of incremented or decremented duty cycle adjusted clock signals;

generating a ~~third control signal or a fourth~~ second set of control signals as a function of the second programmed instruction;

selecting the generated one of the plurality of incremented or decremented duty cycle adjusted clock signals as a function of the ~~third control signal or the fourth~~ second control signals; and

outputting the selected one of the plurality of incremented or decremented duty cycle adjusted clock signals.

32. (Original) The method of claim 31, further comprising:

multiplexing the outputted incremented or decremented duty cycle adjusted clock signal.

33. (Original) The method of claim 31, wherein the input clock signal is a logic signal of a pulse type waveform that switches from low to high and then from high to low with a fixed repetition pattern in time.

34. (Original) The method of claim 33, wherein the pulse type waveform comprises high and low signals in each clock cycle.

35. (Original) The method of claim 31, wherein inputting the first programmed instruction for selecting one of the plurality of incrementing or decrementing separations between the raising edge and the falling edge of the input clock signal further comprises:

storing the first and second programmed instruction in associated memory elements of the integrated circuit.

36. (Original) The method of claim 35, wherein in storing the first and second programmed instruction in memory elements, the memory elements comprise devices selected from the group consisting of registers and flip-flop circuits.

37. (Original) The method of claim 31, further comprising:

generating the input clock signal using an oscillator, wherein the input clock signal has the raising edge and the falling edge in each clock cycle; and

inputting the clock signal into the integrated circuit.

38. (Original) The method of claim 37, wherein in generating the input clock signal, the input clock signal comprises a 50% duty cycle.

39. (Original) A method of adjusting duty cycle of an input clock signal in an integrated circuit, comprising inputting first and second programming instructions into one of a plurality of edge-triggered circuits to select one of a series of plurality of incremental or decremental duty cycle adjust circuits to adjust the duty cycle of a clock signal as a function of the first and second programming instructions.

40. (Original) The method of claim 39, further comprising:

generating the input clock signal using an oscillator, wherein the input clock signal has the raising edge and the falling edge in each clock cycle; and

inputting the clock signal into the integrated circuit.